

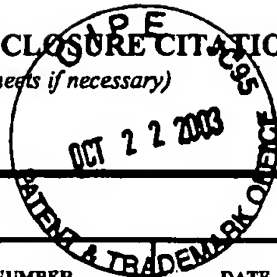
ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	SELF-ALIGNED DRAIN/CHANNEL JUNCTION IN VERTICAL PASS TRANSISTOR DRAM CELL DESIGN FOR DEVICE SCALING						
 Application Number : Confirmation Number: First Named Applicant: Geng Wang Attorney Docket Number: FIS920030209US1 Art Unit: Examiner: Search string: (6414347 or 6440793 or 20020096219).pn							
 US Patent Documents Note: Applicant is not required to submit a paper copy of cited US Patent Documents							
init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
T.D	1	6414347	2002-07-02	Divakaruni	—	—	
T.D	2	6440793	2002-08-27	Divakaruni	—	—	
 US Published Applications Note: Applicant is not required to submit a paper copy of cited US Published Applications							
init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
T.D	1	20020096219	2002-03-11	Chidambarrao	—	—	
 Signature							
Examiner Name				Date			
T. DANG				12/13/04			

INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)



Docket Number (Optional)

FIS920030209US1

Application Number

10/604,731

Applicant(s)

Geng Wang, et al.

Filing Date

8/13/03

Group Art Unit

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

T.D		"Vertical Pass Transistor Design For Sub-100nm DRAM Technologies" K. McStay, et al., Proceedings 2002 Symposium on VLSI Technology, Section 18.3, pp 180-181 June 11, 2002

EXAMINER

T. DAWG

DATE CONSIDERED

12/13/04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.